



A low cost capacitive bridge based on voltage drop balance

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ABSTRACT

The proposed bridge has a simple analog design featuring few components and may be implemented inexpensively at any laboratory. Yet, it is characterized by a low input stray capacitance (1 pF in the prototype with margin for improvement) and a very good accuracy, in terms of measurement uncertainty and repeatability: the method of balancing successive readings of the voltage drops across the “capacitor under test” and a reference resistor uses at best the external voltmeter in terms of measurement accuracy and avoid the need for a voltage reference and related stability issues.

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1. Introduction

The design and development of this bridge stemmed from the need of accurate measurement of SMD (Surface Mounting Device) capacitors, to be used in different applications, such as analog filters. The method must be simple and low cost and must use instruments available in a normal laboratory. Several constraints of other measurement methods must be avoided: no reference capacitors (like in AC bridges or other realizations [1,2]), no switched capacitors circuits and no complex digital architectures [3,4]. The approach is very simple and similar to the operation of LCR meters [5]: a voltage divider is made of a reference resistor R_k (k indicates the element of the array of selectable resistors that implement the scale change) and the unknown capacitor C_x (the capacitor under test or c.u.t.). Then the voltage drops across the two elements are compared and made equal in amplitude on an external voltmeter by adjusting the test frequency. There is no comparison against an external voltage reference, thus avoiding any stability issues, but two approximately equal voltages are read with the same voltmeter within a few seconds, minimizing uncertainty.

Circuit components are few to reduce circuit complexity, to ease circuit realization and to keep the cost low. The proposed circuit wants to be an effective solution for accurate capacitance measurement and should be compared to much more expensive LCR bridges [5], for which the following reference performances may be outlined: 0.1–0.6% accuracy, depending on the frequency, the applied voltage level and the order of magnitude of the impedance of the component under test; almost unlimited range of capacitance values; 6–12 thousands Euros price.

2. Bridge architecture and measurement procedure

The general scheme is shown in Fig. 1. It includes:

- (i) an input block represented by the OA that decouples the variable frequency generator from the rest of the bridge;
- (ii) a voltage divider with the array of selectable resistors R_k and the unknown capacitor under test C_x ;
- (iii) a switch that exchanges the polarity of the applied signal and allows the comparison of the two voltage drops;
- (iv) a voltage buffer that couples the external voltmeter to the voltage divider and that is designed for low input capacitance and high input impedance; it is a

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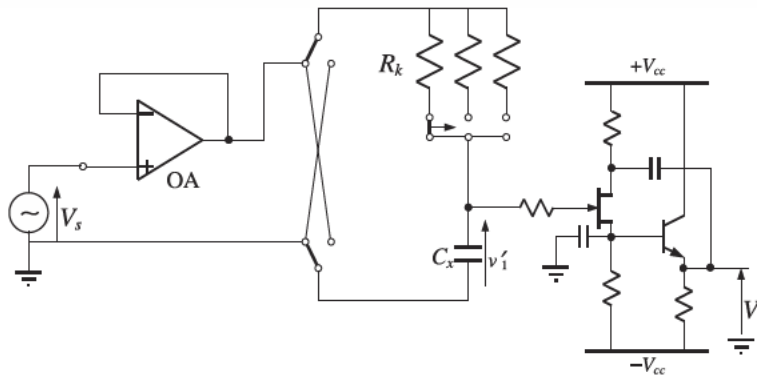


Fig. 1. Capacitance bridge diagram.

source follower input stage with an emitter follower output buffer using a feedback capacitor for reduction of the effective C_{gd} term seen at the input gate, as explained later in this section.

The measurement procedure is quite straightforward:

- (1) select the capacitance scale by turning a knob that selects the resistor R_k , thus setting the reference real impedance with which the capacitive reactance under measurement is compared;
- (2) select the input voltage level to set the voltmeter in the preferred voltage scale (normally $1 V_{ac}$);
- (3) read two voltages V_{up} and V_{dn} by switching up and down the polarity of the applied signal; the switching operation is manual in this implementation, but may be made automatic using a MOS (Metal Oxide Semiconductor) integrated switch with adequately low and stable channel resistance, not to represent a source of error and uncertainty;
- (4) adjust the signal frequency f_s until $V_{up} = V_{dn}$ at the desired reading accuracy, within an acceptable flicker of the least significant digit or digits;
- (5) C_x is then calculated using the following relationships.
- (6) Let us consider the amplitudes of the voltages V_{up} and V_{dn} looking at the amplitude of the voltages appearing on the two voltage dividers formed by reversing the signal polarity. The different phase of the real and capacitive voltage drops does not influence the operation, since the two voltages in up and down configurations are read separately on the voltmeter.

$$\begin{aligned}
 V_{up} &= \frac{R_k}{R_k + j2\pi f_s C_x} V_s \\
 V_{dn} &= \frac{j2\pi f_s C_x}{R_k + j2\pi f_s C_x} V_s
 \end{aligned}
 \tag{1}$$

By equating the two voltages $V_{up} = V_{dn}$, and thus simplifying the two sides of the equation, leaving the numerators, we obtain simply.

$$\frac{1}{2\pi f_s C_x} R_k
 \tag{2}$$

that gives 40.81 nF/kHz at $R_k = 3900 \text{ }\Omega$ or $10.46 \text{ nF/kHz/k}\Omega$.

The range of the input signal frequency f_s has been preliminarily set to $[0.1, 100] \text{ kHz}$ as a trade off between the low capacitance values under measurement and the correct frequency range for the voltmeter and its best declared accuracy. However, any desensitization of the voltmeter at high frequency is of no or little consequence in the determination of C_x , related only to the balancing condition of the two successive readings in up and down conditions. Moreover, the two successive readings are not affected by any medium or long term drifts, and for this reason the attention is focused on short term accuracy, identified in the "sinewave transfer accuracy" term appearing in the multimeter datasheet [8]. If the repetition of the measurement of the same capacitor under test (taken as reference) over a long period of time is considered, then again the short term accuracy comes into play since the determination of its value is always made by comparison of two almost equal voltages over a time interval of a few seconds.

The circuit elements that influence the operation of the bridge and hence the accuracy of the determination of C_x have been identified.

- (1) Nonideal behavior of R_k in terms of parasitic elements, namely series inductance L_k and shunt capacitance C_k : for the considered frequency range, L_k gives a series term lower than $1 \text{ m}\Omega$ (in series to the switch resistance and to the Operational Amplifier driving impedance) and C_k a parallel term larger than $3 \text{ M}\Omega$. For a target accuracy lower than 0.1% , the R_k values have been limited in the prototype to $10 \text{ } 70,000 \text{ }\Omega$ approximately, with the most sensitive scale using a $78,000 \text{ }\Omega$ resistor with a 0.12% error. Of course, a significant improvement of the overall parasitic capacitance is obtained if the larger value resistors are built with a series connection of smaller ones or if the systematic error of the shunting parasitic capacitance is compensated for.
- (2) Finite input impedance of the output voltage buffer: it consists of a source follower FET (Field Effect Transistor) followed by a second emitter follower stage with a feedback capacitor on the FET drain to reduce the effect of C_{gd} on the total input capacitance; the input capacitance is thus formed approximately by the C_{gs}

alone. The measurements done on the prototype confirm that the total parasitic capacitance is quite constant and given by 1.0 pF (see end of Section 3).

- (3) Any effect of the switch nonidealities (finite resistance and contact noise) is made negligible by the use of both the very low Operational Amplifier driving impedance and the input signal voltage level at about 0.8 V, in order to keep the signal generator in the best range to limit distortion, while ensuring the correct scale of the voltmeter.

Last, test voltage levels higher than those normally specified for capacitance measurement ($<2 V_{ac}$) may be obtained by increasing the generator signal and possibly the supply voltage V_{cc} , while keeping it below the maximum ratings of Operational Amplifiers and transistors (about 10–15 V). A further increase may be obtained if high voltage components are selected and the generator signal is amplified by the Operational Amplifier itself. In this way it will be possible also to test the capacitor C_x behavior at different voltage levels, thus evaluating any nonlinearity and nonidealities.

3. The prototype

A prototype has been built with the following components (a picture is reported in Fig. 2).

The choice of the resistors $R_k = 390 \Omega, 3900 \Omega, 39,000 \Omega$ and $78,000 \Omega$ was dictated by the values of the capacitors in stock in the laboratory for the realization of some instruments and prototypes, and they correspond approximately to the following capacitance scales: 4 μF , 400 nF, 40 nF, 20 nF (see Table 1). An additional 39 Ω allows to reach the 40 μF scale and, together with a reduction in the signal frequency down to 40 Hz, the 100 μF full scale. A 3.9 Ω is not precluded, but as already for the 39 Ω case self heating and Operational Amplifier output current limit must be taken into account.

The selected Operational Amplifier is an EL 2045 [6] in unitary gain configuration (voltage buffer), that ensures a negligible driving impedance; other Operational Amplifiers

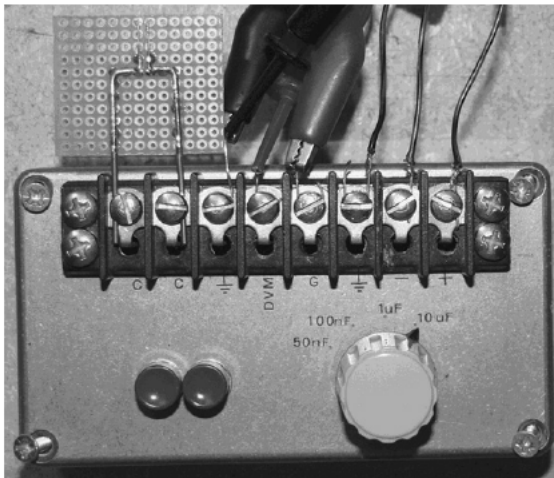


Fig. 2. Picture of the prototype.

Table 1
Capacitance ranges for the assigned frequency interval.

$R_k (\Omega)$	C_{min} @ 100 kHz	C_{max} @ 100 Hz
390	4.08 nF	4.08 μF
3900	408 pF	408 nF
39,000	40.8 pF	40.8 nF
78,000	20.4 pF	20.4 nF

exist from different manufacturers with the required characteristics, but this one was already available and features a 12 MHz full power bandwidth and a 75 mA typical output short circuit current, ensuring the driving capability needed for very large capacitors and/or very high test frequency. The switch is a C&K with silver contacts to avoid changes due to oxidation.

The FET is a 2N3819 [7] in TO92 package (selected for mounting convenience) with not a particularly low C_{gs} , so that an improvement is expected by the selection of low capacitance FET in SMD package.

The total equivalent parasitic input capacitance C_p conveys all the parasitic elements of the bridge circuit. It could have been measured with an external capacitance bridge connected to the input terminals (but it could be unavailable in most laboratories) or with the same proposed instrument taking a reading with the open input terminals (that represents an out of range reading, with very high frequency above voltmeter range and with increase in generator distortion). Rather, a technique was used based on three readings and the following simple reasoning. After selecting two capacitors C_1 and C_2 of conveniently low value (so that the parasitic capacitance C_p is a significant fraction and is not so affected by the unavoidable round offs), three readings are made with the usual measurement procedure for the following choices: C_1, C_2 and $C_{12} = C_1 + C_2$ (in parallel). The parasitic capacitance C_p is present in parallel in all readings, so that $C'_1 = C_1 + C_p, C'_2 = C_2 + C_p, C'_{12} = C_1 + C_2 + C_p$; then C_p is determined as $C_p = C'_1 + C'_2 - C'_{12}$. The measured values are $C_1 = 11.4$ pF, $C_2 = 11.3$ pF, $C_{12} = 21.7$ pF, so $C_p = 1.0$ pF.

4. Type B and Type A uncertainties

From the description of the bridge elements and of the measurement procedure, it is possible to draw some considerations on the accuracy and proceed to the quantification of the uncertainty of the prototype.

The main sources of error have been identified and Type B uncertainty is considered in the following (a voltmeter brand and model is used to derive a numeric example).

- (1) The output voltmeter and the AC true rms voltage accuracy influence directly the balance of the two voltages V_{up} and V_{dn} ; taking the amplitude of the signal V_s equal to the full scale of the multimeter, a relative error ϵ_V on the balance of the two readings leads to the following expression:

$$\left| \frac{R_k}{R_k + \frac{1}{j2\pi f_s C_x}} \right| \left| \frac{\frac{1}{j2\pi f_s C_x}}{R_k + \frac{1}{j2\pi f_s C_x}} + \epsilon_V \right| \tag{3}$$

Since at balance the two terms R_k and $1/(j2\pi f_s C_x)$ are nearly equal, the absolute value of the denominators is $\sqrt{2}R_k$; the relative error ε_V on the voltage balance produces a relative error $\varepsilon_Z = 1.41\varepsilon_V$ in the equality (2) and thus in the determination of the value of the capacitor under test C_x .

A HP 34401A [8] was used for the presented tests and the “sinewave transfer accuracy” (specified by the manufacturer at $\pm 4\sigma$) is 0.002% for the 10 Hz–50 kHz and 0.005% for the 50–300 kHz frequency ranges; the conditions assumed by the manufacturer’s in the datasheet are ensured by the choice of the signal level close to full scale, the sinusoidal feeding signal, the constant frequency and the successive readings performed over a few seconds, so that it is a short term accuracy, rather than a medium or long term accuracy.

- (2) The signal generator must only be accounted for the f_s value, that for digitally synthesized generators, such as the HP 33120A, is very accurate and its uncertainty contribution negligible; in order to use also analog signal generators, the frequency may be read by the multimeter itself and the accuracy of the HP 34401A is 0.01% (specified again by the manufacturer at $\pm 4\sigma$).
- (3) The accuracy of the value of the reference resistor R_k has a direct influence on the determination of C_x ; it may be determined with great accuracy with a resistance bridge (such as a Wheatstone bridge) or with a direct measurement using the same multimeter, attaining a variable accuracy, depending on the resistor value and the instrument used, better than 0.002% [8] for a four wire measurement, again specified by the manufacturer at $\pm 4\sigma$. On the contrary, the change of the resistance versus time and environmental conditions is in relationship with the type of resistor and highly depends on the implementation. Low temperature coefficient and high stability resistors are available for the considered range of values (from a fraction of k Ω up to a 100 k Ω); if the temperature is stabilized the overall change is less than approximately 10 ppm.
- (4) The internal parasitic elements, to be considered in particular for extreme values of the input frequency and of the reference resistor R_k , may be compensated for in different ways: (i) a corrective multiplying factor may be applied a posteriori directly on the C_x values; for the extreme case of a 10 pF capacitor under test requiring a signal frequency of 204 kHz, we obtain 1.56 M Ω of reactance (assuming 0.5 pF of parasitic capacitance) in parallel to the 78,000 Ω resistor, so a worst case error of 0.12%; (ii) the total parasitic capacitance across the resistor R_k may be minimized by an optimized design: with a series connection of six 13,000 Ω resistors (to get the 78,000 Ω value) this error term drops immediately to 0.02% or less; it is underlined that this kind of deterministic errors is significant only above 100 kHz for the lowest scale (for the second resistor in the array equal to 39,000 Ω we have only a 75 ppm error for a single resistor and 2 ppm for six resistors in series).

So, Type B uncertainty is dominated by the frequency reading accuracy of the used multimeter, stated by the manufacturer equal to 0.01% at $\pm 4\sigma$ (so, 0.005% at $\pm 2\sigma$, that is with a $k = 2$ coverage). If the signal generator is digitally synthesized and the frequency reading accuracy term is thus not relevant, then the overall Type B uncertainty is the combination of the terms considered at points 1 (0.0014% or 0.0035% for the two frequency ranges), 3 (0.001% for both resistance measurement and resistance change) and 4 (a variable accuracy that can be brought to 10 ppm with a little design effort within the 100 kHz frequency range). The overall uncertainty may be then estimated ranging between about 20 and 40 ppm.

Type A uncertainty has been evaluated together with repeatability for a NP0 100 pF ceramic capacitor in SMD 0805 package, used as reference. The expected result is about some tens of ppm and in this range the piezoelectric effect comes into play: for this reason two sets of measurements have been collected. For each measurement the entire procedure is repeated: the capacitor under test is inserted, then after the selection of the scale resistor, the repeated readings with signal reversal are made by adjusting the signal frequency, until the two voltages are equal at the desired reading accuracy, the voltage amplitude and frequency values are written on the test sheet and then the capacitor under test is removed.

The first set is characterized by a weak and not so constant mechanical force at the electric contacts, that gives the most uncertain results, but maybe closer to the real capacitance value. Type A uncertainty in terms of 2σ dispersion is about 200 ppm on a series of 10 measurements (over a 10 min time interval) with a mean capacitance of 101.227 pF (including stray capacitance).

The second set has a stronger mechanical force obtained with two spring contacts, that is however better under control and for this reason constant. The maximum spread of values is 5 ppm on a series of 10 measurements (over a 10 min time interval) and the mean capacitance is 101.209 pF (including stray capacitance). This value is compatible with the 10 ppm accuracy estimated as Type B uncertainty for the case of a digitally synthesized signal and 100 pF scale.

The difference between the two mean values is only 18 fF or 180 ppm.

5. Conclusions

A simple inexpensive bridge for capacitance measurement with low component count has been presented, suitable for lab testing of capacitors where high accuracy is required (for example analog filter elements, voltage dividers, etc.). The accuracy depends not only on the internal circuit, but also on the characteristics of the external signal generator and voltmeter. It is shown that for the considered interval of test frequency values (0.1–100 kHz), the internal sources of error may be kept well below 0.1% and, if adequately compensated, the limiting accuracy is that of the external voltmeter. The comparison of two voltages of almost equal magnitude to reach equilibrium ensures that the voltmeter accuracy is the best attainable

(defined for the adopted voltmeter as “sinewave transfer accuracy”). The Type A uncertainty has been evaluated with a reference capacitor observing a 5 ppm spread of values for 10 repeated measurements over a 10 min interval. For very accurate measurements the test jig arrangement to hold SMD components must be accurately designed in order to avoid any piezoelectric effect, as it is for more expensive LCR bridges.

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